REMARKS

Favorable consideration of this application is respectfully requested.

Claims 1-41 are currently active in this case. Claim 38 has been amended by way of the present amendment. The amended claim is supported by the specification and claims as originally submitted and no new matter has been added.

In the outstanding Official Action, Claim 38 was rejected under 35 U.S.C. §112, second paragraph as being indefinite; and Claims 1-41 were rejected as being unpatentable under 35 U.S.C. §103(a) over *Gilbertson* (U.S. Pat No. 6,510,405 B1).

Claim 38 has been amended to broaden its scope. Amended Claim 38 is believed to be definite under 35 U.S.C. §112, second paragraph. If the Examiner disagrees, the Examiner is invited to call the undersigned who will be happy to work with the Examiner in a joint effort to describe mutually satisfactory claim language.

Applicants respectfully traverse the rejection of Claim 1 under 35 USC 103 as being unpatentable over *Gilbertson*. Claim 1 recites:

> ***A method for performing a simulation process for a design using a set of existing stimuli that are specified in a predetermined sequence, the method comprising the steps of:***
>
> ***dividing all possible design states for the design into a plurality of validation regions;***
>
> ***recording simulation history for all the validation regions during the simulation process;***

generating a new set of stimuli by examining the existing stimuli based on the simulation history; and

performing the simulation process using the new set of stimuli.

However, *Gilbertson* fails to teach or suggest similar subject matter.

Applicants respectfully note that *Gilbertson* is a method for selectively displaying signal values generated by a logic simulator. The signal values are selected for display (or other listing). For example, the displayed (listed) values may be any of register or counter outputs (e.g. output signals A, B, C, or D in Fig. 3A), a logic signal (e.g., overflow signal (OVR 68), Fig. 3A), etc. The displayed (listed) values are essentially information/knowledge used to evaluate circuit operations as would normally be performed to "debug" a circuit design (e.g., see *Gilbertson* col. 9, lines 26-31 "success of debugging many design problems is dependent on the knowledge of the sequence and type of events that occurred just prior to the unexpected logic behavior or error condition," and other references in *Gilbertson* to debugging operations).

Gilbertson provides detailed discussion about how the various signals may be displayed, and provides rather complex scenarios as to when the signals are to be displayed. For example, at col. 9, lines 41-48, *Gilbertson* discusses listing the values only when the values are in a predetermined state (e.g., Fig. 4, step 88 "Identify a time when one or more of the signals are in a predetermined state" and step 90, "Display predetermined set of identified signal values at a time that is related to the identified time.").

Applicants admit that *Gilbertson's* displayed or listed signal values is a type of historical data with regard to a simulation run. However, it should be noted that *Gilbertson* is only directed toward determining that historical data at specific

points, or at specific points during specific times of the simulation. Therefore, *Gilbertson* only teaches a mechanism for retrieval and display (or storage) of signal values that occur within a simulation. And, the signal values (or historical data) are the simulation itself, not stimuli data provided to the simulation. Furthermore, the signal values displayed/stored are directed toward debugging the circuit being simulated and are not applied to generation, transformation, or other operations of stimuli data.

In contrast, Claim 1 includes steps for generating a specific product for use by a simulation. For example, Claim 1 includes the steps of "generating a new set of stimuli by examining the existing stimuli based on the simulation history." Claim 1 also includes the step of "performing the simulation process using the new set of stimuli." However, *Gilbertson* fails to teach or suggest the same.

Applicants respectfully traverse any assertion that *Gilbertson's* virtual history stack and discussions related thereto teach or suggest "to produce corrective action and valid stimulus test data" (e.g., at Fig. 5, col. 6, lines 14-44, col. 8, lines 33-60). In contrast, Fig. 5 is a flow chart that illustrates logic to display or otherwise list selected signal data at selected times (e.g., if a logical operation is true (step 98), then display the identified signals (step 100), otherwise try the next interval (if any) (step 106).

Furthermore, Col. 6, lines 14-44 only describe retrieval of signal values, and updating previously retrieved signal values with newly retrieved signal values. Updates of previously retrieved signal values are performed based on a specific condition (e.g., signal definition 10 identifies when signals should be updated). However, this only describes updating of the simulation history itself, which is tantamount to simply re-capturing the simulation data. And, neither capture nor re-capture of signal data can be equated to "generating a new set of stimuli data ..." as claimed in Claim 1. Furthermore, Applicants respectfully note that stimuli data is entirely different than simulation history data regardless of when or how the

history data is captured. Therefore, *Gilbertson's* updating (or re-capture) of signal values neither teaches nor suggests Applicant's steps of generating a new set of stimuli data and performing a simulation with the new set of stimuli.

Further yet, Col. 8, lines 33-60 also only describes the capture and update of selected signal values based on specific logic conditions. Fig. 3B is a listing of captured signal values over times 10 than 60 that occur within the circuit of Fig. 3A. However, Claim 1 recites generating new stimuli data based on historical data.

Applicants also respectfully traverse any assertion that either Col. 8 or Col. 9 of *Gilbertson* provides any further disclosure that would either anticipate or make obvious Claim 1. Applicants have admitted that *Gilbertson* teaches collection and/or storage of historical data (e.g., "virtual history stack," etc.). However, historical data of a circuit does not suggest generation of stimuli data based on simulation history or other historical data. Furthermore, *Gilbertson* provides no suggestion to perform a simulation using the newly generated stimuli data.

Therefore, Applicants respectfully submit *Gilbertson* fails to teach or suggest significant features specifically claimed in Claim 1. And, absent those features, Claim 1 cannot be considered obvious over *Gilbertson*. Accordingly, Applicants respectfully submit that Claim 1 is patentable.

Applicants also respectfully traverse the rejection of Claim 4 under 35 USC103 as being unpatentable over *Gilbertson*. Claim 4 recites:

> ***A method for performing a simulation process for a design using a set of existing stimuli that are specified in a predetermined sequence, the method comprising the steps of:***
>
> ***dividing all possible validation states for the design into a plurality of validation regions;***

recording simulation history for each of the validation regions during the simulation process;

taking a stimulus from the existing stimuli for performing a next simulation step for a current validation region, wherein the stimulus is taken in an order specified by the predetermined sequence;

examining the simulation history for the taken stimulus in the current validation region; and

transforming the taken stimulus into an interesting stimulus based on the simulation history.

However, *Gilbertson* fails to teach or suggest similar subject matter.

As discussed above, *Gilbertson* fails to teach or suggest generation of new stimuli data based on the simulation history, or performing a simulation process with the new set of stimuli data. In addition, after careful review of *Gilbertson* as a whole, and particularly the above cited sections (e.g., Figs. 3A/3B, 4, and 5, and cols. 6, 8, 9, et al), Applicants have not been able to find any suggestion of, for example, "transforming the taken stimulus into an interesting stimulus based on the simulation history," as claimed in Claim 4. Therefore, Applicants respectfully submit that Claim 4 cannot be considered obvious over *Gilbertson* because, again, important claim limitations are neither taught nor suggested by *Gilbertson*. Accordingly, Applicants respectfully submit that Claim 4 is also patentable.

Applicants respectfully note that the remaining independent claims also contain limitations that are similarly absent from *Gilbertson*. For example, Claim 10 recites "generating an interesting stimulus in accordance with the stimulus specification based on the simulation history of the validation regions." Claim 13 recites "transforming the taken stimulus into an interesting stimulus based on the simulation history." Claim 19 recites "means for generating a new set of stimuli by examining the existing stimuli based on the simulation history." Claim 22

recites "means for transforming the taken stimulus into an interesting stimulus based on the simulation history." Claim 28 recites "means for generating an interesting stimulus in accordance with the stimulus specification based on the simulation history of the validation regions." And, Claim 31 recites "means for transforming the taken stimulus into an interesting stimulus based on the simulation history." Applicants also respectfully note that the above claims each contain other limitations that further distinguish *Gilbertson*. However, since each claim contains at least one limitation that fully distinguishes it from *Gilbertson*, Applicants respectfully submit that they cannot be considered obvious in view of *Gilbertson*. Accordingly, Applicants respectfully submit that Claims, 10, 13, 19, 22, 28, and 31 are also patentable over the cited art.

Based on the patentability of independent Claims 1, 4, 10, 13, 19, 22, 28, and 31, Applicants further respectfully submit that dependent Claims 2-3, 5-9, 11-12, 14-18, 20-21, 23-27, 29-30, and 32-41 are also patentable.

Consequently, no further issues are believed to be outstanding, and it is respectfully submitted that this case is in condition for allowance. An early and favorable action is respectfully requested.

Respectfully submitted,

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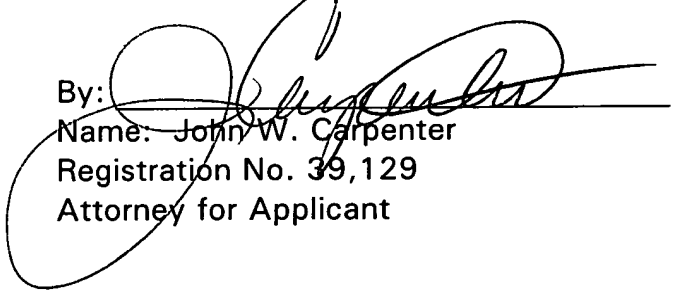
By: 
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